REMARKS

Response to Examiner's Response to Arguments

The Examiner stated that Applicant's arguments filed February 2, 2006 have been fully considered, but the arguments regarding the drawings and regarding claims 1-20 are not considered to be persuasive. Following are the Applicant's responses thereto, showing that the previous arguments were valid and that the present application is therefore in condition for allowance.

Drawings:

Concerning the drawings, the Examiner has stated in several different ways that the drawings would be better if they contained labels. However, the Examiner has not provided a single reason why labels are necessary or essential, which is the explicit standard set forth in the Rules. (See 37 CFR §§1.84(o) and 1.83).

The Examiner has even asserted that the drawings are "defective" because they contain no written labels, and that "the examiner cannot determine what components or whether any of the components are shown".

However, the present Examiner is the same Examiner who approved the identical drawings and specification in the corresponding PCT application for this invention. Therefore, contrary to the Examiner's assertions in the present application, the Examiner has already established on the record that the Examiner can understand the drawings, and that written drawing labels are therefore not NECESSARY for understanding the drawings, in accordance with the Rules.

Inasmuch as the continued drawings requirement therefore appears to be administrative arbitrariness, withdrawal of the requirement is respectfully requested.

Claims:

The Inventor in the present application has provided technical responses, presented immediately below, in reply to the Examiner's numbered response paragraphs 8–19.

> "8. Kelkar's invention doesn't function with a data input. Combining Ferraiolo and Kelkar doesn't give a jitter measurement solution. The combination would be inoperative as Kelkar's invention needs a clock to be

measured. Block 66 of Fig.4 says "CAPTURE VALUE OF MEASURED SIGNAL AT TRANSITION EDGES OF DELAY SIGNALS". With a data signal there may be no transition of the measured signal near any of the 'delay signals' so a reading of 0000 or 1111 will be measured in this case. This will be indistinguishable from times when the real reading is 0000 or 1111."

Concerning paragraph 9, the inventor indicated that he felt that the Examiner does not understand what a digital capacitor is. It is respectfully pointed out by the undersigned that a digital capacitor is in fact an analog device. Digital capacitors are so-named because they incorporate a digital voltmeter, but the electrical performance is like that of any other capacitor – namely, analog. Here, for example, is an Internet link that the Examiner is invited to consult on this point:

http://www.electronixwarehouse.com/car/accessories/capacitors.htm

(Please note the "PLEASE NOTE" item at the bottom of the Internet-linked page, which states, "The term "digital" refers to a built-in digital voltmeter on the capacitor. All capacitors are inherently analog devices, otherwise.").

"10. We still claim the Kelkar calibration is unnecessary. Our invention uses the delay elements as they come, and uses a method to calibrate what each of the delay elements actual delay is. This is simpler and easier to construct than the Kelkar invention."

"11. Kelkar and Yanagisawa's inventions are not able to be combined to make an improved jitter measurement invention that digitally measure jitter on a data signal."

"12. The examiner has not understood our point. No amount of filtering before or after gets away from the fact that Kelkar produces a measurement of the probability density function of the jitter. This is not sufficient to meet the demands of a jitter measurement system for random data. It provides no indication of the frequency component of the jitter, only amplitude. Our invention does both frequency and jitter measurement."

13. [No comment.]

> "14. Yanagisawa's invention clearly contains a lot of analog circuitry. Figs. 3, 4, 5, and 6 clearly show analog circuits. Fig.12 shows current sources, sample and hold, an amplifier, and an ANALOG to digital converter."

> "15. It is obvious to one trained in the art AFTER reading the description of our invention that jitter measurement occurs on every transition."

Comment by the undersigned: the point addressed here has to do with the fact, as stated in the prior Response, that one of ordinary skill in the art considering the digital teachings of the present invention would not look to Yanagisawa. The statement is therefore very relevant to the rejection of claim 1 because the rejection is a §103 rejection and Yanagisawa is not a relevant citation for the many reasons given, including this one.

> "16. We claim to 'digitally' measure jitter. This precludes the use of timing capacitors..."

Ditto concerning the relevance of this point. Also, the claim, as amended, is very clear that the core functions that are recited are done "digitally", precluding the use of timing capacitors as stated by the Inventor.

> "17. ...and comparators."

> "18. We would not recite a limitation in our invention. The invention does not need or use a counter as needed by Yanagisawa. This shows the invention is different from Yanagisawa."

And hence, once again, Yanagisawa is not relevant to the present invention and would not be consulted by one of ordinary skill in the art seeking to combine prior art to accomplish the present invention.

> "19. Yanagisawa only detects the 'accumulation' of widths of many pulses. Our invention detects the positions of each and every edge which is important for measuring peak jitter. If one and only one edge exceeded a value, Yanagisawa's invention would not detect it."

Accordingly, it is clear that the prior responses filed on January 5, 2006, fully and patentably distinguish the present invention from the cited prior art. Reconsideration and allowance are therefore respectfully requested.

Drawings

The Examiner stated that the drawings are objected to under 37 CFR 1.83(a).

For the reasons stated above, withdrawal of this objection is appropriate and is therefore respectfully requested.

Claim Rejections - 35 USC §103

Claims 1, 2, 3, and 4 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kelkar et al. (U.S. Patent No. 5,663,991, hereinafter "Kelkar") in view of Yanagisawa et al. (U.S. Patent No. 6,528,982, hereinafter "Yanagisawa").

For the reasons stated above, corroborating the reasons previously presented in the Response filed January 5, 2006, withdrawal of this rejection is appropriate and is therefore respectfully requested.

Claims 6-9, and 11-14 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kelkar et al. (U.S. Patent No. 5,663,991, hereinafter "Kelkar") in view of Yanagisawa et al. (U.S. Patent No. 6,528,982, hereinafter "Yanagisawa") and further in view of Sunter et al. (U.S. Pub. No. 2005/0069031, hereinafter "Sunter").

For the reasons stated above, corroborating the reasons previously presented in the Response filed January 5, 2006, withdrawal of this rejection is appropriate and is therefore respectfully requested.

Claims 16-19 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kelkar et al. (U.S. Patent No. 5,663,991, hereinafter "Kelkar") in view of Yanagisawa et al. (U.S. Patent No. 6,528,982, hereinafter "Yanagisawa") and further in view of Sunter et al. (U.S. Pub. No. 2005/0069031, hereinafter "Sunter") and further in view of IEEE Design and Test of Computers, "FPGA and CPLD Architectures: A Tutorial".

For the reasons stated above, corroborating the reasons previously presented in the Response filed January 5, 2006, withdrawal of this rejection is appropriate and is therefore respectfully requested.

Claim 5 is rejected under 35 U.S.C. §103(a) as being unpatentable over Kelkar et al. (U.S. Patent No. 5,663,991, hereinafter "Kelkar") in view of Yanagisawa et al. (U.S. Patent No. 6,528,982, hereinafter "Yanagisawa") and further in view of Jungerman et al. (U.S. Pub. No. 2004/0146097, hereinafter "Jungerman").

For the reasons stated above, corroborating the reasons previously presented in the Response filed January 5, 2006, withdrawal of this rejection is appropriate and is therefore respectfully requested.

Claims 10 and 15 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kelkar et al. (U.S. Patent No. 5,663,991, hereinafter "Kelkar") in view of Yanagisawa et al. (U.S. Patent No. 6,528,982, hereinafter "Yanagisawa"), further in view of Sunter et al. (U.S. Pub. No. 2005/0069031, hereinafter "Sunter") and further in view of Jungerman et al. (U.S. Pub. No. 2004/0146097, hereinafter "Jungerman").

For the reasons stated above, corroborating the reasons previously presented in the Response filed January 5, 2006, withdrawal of this rejection is appropriate and is therefore respectfully requested.

Claim 20 is rejected under 35 U.S.C. §103(a) as being unpatentable over Kelkar et al. (U.S. Patent No. 5,663,991, hereinafter "Kelkar") in view of Yanagisawa et al. (U.S. Patent No. 6,528,982, hereinafter "Yanagisawa"), further in view of Sunter et al. (U.S. Pub. No. 2005/0069031, hereinafter "Sunter"), further in view of IEEE Design and Test of Computers, "FPGA and CPLD Architectures: A Tutorial", and further in view of Jungerman et al. (U.S. Pub. No. 2004/0146097, hereinafter "Jungerman").

For the reasons stated above, corroborating the reasons previously presented in the Response filed January 5, 2006, withdrawal of this rejection is appropriate and is therefore respectfully requested.

Conclusion

In view of the above, it is submitted that the claims are in condition for allowance and reconsideration of the rejections is respectfully requested. Allowance of claims 1–20 at an early date is solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including any extension of time fees, to Deposit Account No. 50-0374 and please credit any excess fees to such deposit account.

Respectfully submitted,

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